An Improved iUPQC fed with a novel FLC Controller to Provide Additional Grid-Voltage & power Regulation

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***Abstract*—This so as to meet PQ standard breaking points, it might be important to incorporate some kind of remuneration. Advanced arrangements can be found as dynamic correction or dynamic filtering. A shunt dynamic power filter is appropriate for the concealment of negative load impact on the supply network, yet in the event that there are supply voltage defects, an arrangement dynamic power filter might be expected to give full pay. As of late, arrangements in view of adaptable air conditioning transmission systems (FACTS) have showed up. The utilization of FACTS ideas in circulation systems has brought about another era of remunerating gadgets. A fluffy rationale controller based enhanced brought together power quality conditioner (IUPQC) is the augmentation of the bound together power-quality controller (IUPQC) idea at the conveyance level. It comprises of joined arrangement and shunt converters for concurrent remuneration of voltage and current flaws in a supply feeder. The fluffy rationale controller (FLC) sustained IUPQC comprises of one arrangement and one shunt converter. It is associated between two feeders to manage the bus voltage of one of the feeders, while controlling the voltage over a touchy load in the other feeder. In this arrangement, the voltage control in one of the feeders is performed by the shunt-VSC. Be that as it may, since the source impedance is low, a high measure of current would be expected to support the bus voltage in the event of a voltage list/swell which is not plausible. It additionally has low element execution on the grounds that the dc-interface capacitor voltage is directed.**

Keywords— iUPQC, Grid, Fuzzy Logic Controller, FACTS, Power Quality

I. INTRODUCTION

Because of the use of number of electronic parts in businesses, homes and so forth, where these gadgets require top notch energy to work legitimately and in the meantime these are the most in charge of infusion of voltage hangs, swells, sounds and other related unsettling influence in the conveyance framework. Voltage Source Converter based custom power gadgets are progressively being utilized as a part of custom-power applications for enhancing the power quality (PQ) of power dispersion systems. Gadgets, for example, dispersion static compensator (DSTATCOM) and element voltage restorer (DVR) have as of now been talked about widely in [1]. A DSTATCOM can repay the bending and unbalance because of symmetrical and hilter kilter blames in a heap with the end goal that an adjusted sinusoidal current moves through the feeder [2]. It can likewise direct the voltage of a conveyance bus [3], [4]. A DVR can repay the voltage droop/swell and mutilation in the supply side voltage with the end goal that the voltage over a delicate/basic load terminal is superbly regulated[5], [6]. An Interline brought together power-quality conditioner (IUPQC) can play out the elements of both DSTATCOM and DVR [7], [8].The IUPQC comprises of two voltage-source converters (VSCs) that are associated with a typical dc bus. One of the VSCs is associated in arrangement with a dissemination feeder, while the other one is associated in shunt with similar feeder.

In [9], a design called IDVR has been talked about in which two DVRs are associated in arrangement with two separate adjoining feeders. The dc busses of the DVRs are associated together. The IDVR ingests genuine power from one feeder and keeps up the dc interface voltage to relieve 90% (around 0.1 p.u.) voltage hang in the other feeder with adjusted burdens associated in the circulation framework. It is additionally conceivable to interface two shunt VSCs to various feeders through a typical dc connect. The IUPQC comprises of two voltage-source converters (VSCs) that are associated with a typical dc bus.

Another association for an IUPQC with Fuzzy Logic Controller to decrease the THD impressively contrasted with traditional PI controller based voltage source converters. Two feeders, Feeder-1 and Feeder-2, which are associated with two distinct substations, supply the framework loads L-1 and L-2. The supply voltages are indicated byVs1 and Vs2 [1]. It is expected that the IUPQC is associated with two busses B-1 and B-2, the voltages of which are signified by Vt1 and Vt2 individually. Advance two feeder currents are indicated by is1 andis2 while the heap currents are meant by il1 and il2. The heap L-2 voltage is signified by Vt2. The reason for the IUPQC is to hold the voltages Vt1 and Vt2 consistent against voltage hang, swell, issues and music in both of the two feeders. It has been exhibited that the IUPQC can ingest power from one feeder (sayFeeder-1) to Hold Vt2 steady if there should be an occurrence of a list in the voltage Vs2.This can be proficient as the two VSC's are provided by a typical dc capacitor. The dc capacitor voltage control has been talked about here alongside voltage reference era system. Additionally, the cutoff points of achievable execution have been figured. The execution of the IUPQC has been assessed through simulation studies utilizing MATLAB/SIMULINK.

II. STRUCTURE AND CONTROL

The IUPQC consists of two VSCs (VSC-1 and VSC-2) that are connected back to back through a common energy storage dc capacitor Cdc. Let us assume that the VSC-1 is connected in shunt to Feeder-1 while the VSC-2 is connected in series with Feeder-2.An IUPQC connected to a distribution system is shown in Fig.1.

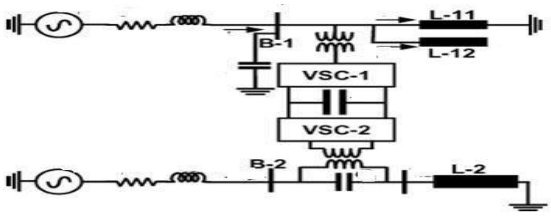

Fig. 1. IUPQC connected in distribution system.

In this figure 1, the feeder impedances are meant by the Pairs (Rs1, Ls1) and (Rs2, Ls2). It can be seen that the two feeders supply the heaps L-1 and L-2. The heap L-1 is expected to have two separate segments—a lopsided part (L-11) and a non-straight part (L-12).The currents drawn by these two burdens are signified byIt11and It22 individually. It is expected that the heap L-2 is a delicate load that requires continuous and managed voltage. The shunt (VSC-1) is associated with bus B-1 toward the end of Feeder-1[3], [4], while the arrangement (VSC-is associated at bus B-2 toward the end of Feeder-2 [5], [6]. The voltages of busses B-1 and B2 and over the delicate load terminal are signified by Vt1 and Vt2 individually. With a specific end goal to achieve these points, the shunt VSC-1 is worked as a voltage controller while the arrangement VSC-2 manages the bus voltage Vt2across the touchy load [1]. The length of Feeder-1 is discretionarily been twice that of Feeder-2.The finish structure of a three-stage IUPQC with two such VSCs is appeared in Fig. 2.

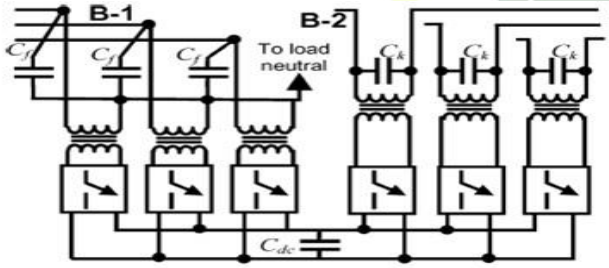

Fig. 2. Complete structure of an IUPQC.

The optional (dispersion) sides of the shunt-associated transformers (VSC-1) are associated in star with the impartial indicate being associated the heap nonpartisan. The optional twisting of the arrangement associated transformers (VSC-2) are straightforwardly associated in arrangement with the bus B-2 and load L-2.The schematic structure of a VSC is appeared in Fig.4. Each of the two VSCs is acknowledged by Three H-connect inverters [10] [11].

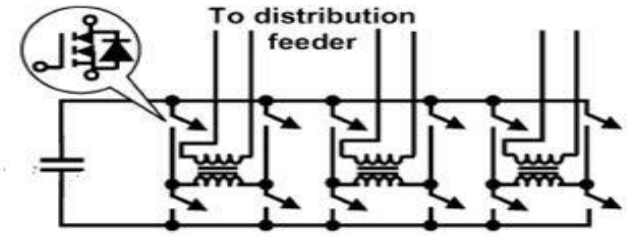

Fig. 3. Schematic structure of VSC.

In this structure, every switch speaks to a power semiconductor gadget (e.g., IGBT) and a hostile to parallel diode as appeared in Fig.3. Every one of the inverters are provided from a typical single dc capacitor Cdc and every inverter has a transformer associated at its yield. A). IUPQC Power System: Block chart and Simulation outline of the power circuit of IUPQC framework are appeared above in fig.4 and fig. 5, comprises of the 3-arm IGBT based inverter and the battery as energy stockpiling framework. The source is 11KV sustained from circulation substation.11 KV is then decreased to 415 V by venture down transformer before interfacing with load. In this study, two sorts of load, Non Sensitive Load and Sensitive load are considered. The LC filter is acquainted with wipe out exchanging swells delivered by the inverter. A blame generator is acquainted purposefully with create voltage symmetrical and Asymmetrical shortcomings at various levels and by differing issue resistance esteem we can infuse music into the framework however a diode rectifier. Hangs and Swells. It can be created inside the 3-Φ framework supply. Here feeder-1 is taken in base side and feeder-2 is taken at top.

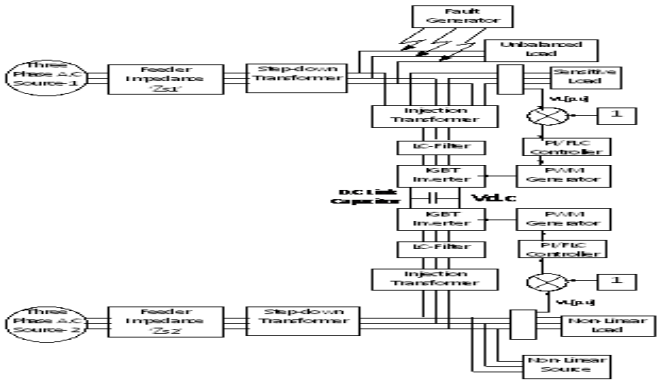

Fig. 4. Block Diagram of IUPQC power circuit.

III. SYSTEM DESCRIPTION

An IUPQC associated with a circulation framework is appeared in Fig. 4. In this figure, the feeder impedances are indicated by the Pairs (Rs1, Ls1) and (Rs2, Ls2). It can be seen that the two feeders supply the heaps L-1 and L-2. The heap L-1 is accepted to have two separate segments an uneven part (L-11) and a non-direct part (L-12). The currents drawn by these two burdens are meant by it11 and it12 individually. We promote expect that the heap L-2 is a delicate load that requires continuous and controlled voltage. The shunt (VSC-1) is associated with bus B-1 toward the end of Feeder-1, while the arrangement (VSC-2) is associated at bus B-2 toward the end of Feeder-2. The voltages of busses B-1 and B2 and over the

touchy load terminal are signified by Vt1 and Vt2 separately. The point of the IUPQC is two-overlay.

- To protect the sensitive load L-2 from the disturbances occurring in the system by regulating the voltage (V_{t2}).
- To regulate the bus B-1 voltage V_{t1} against sag/swell and or disturbances in the system.

With a specific end goal to accomplish these points, the shunt VSC-1 is worked as a voltage controller while the arrangement VSC-2 manages the voltage Vt2 over the touchy load. The framework parameters utilized as a part of the study are given in Table I. The length of Feeder-1 is self-assertively been twice that of Feeder-2. The voltage of bus B-1 and load L-1 currents, when no IUPQC is associated with the dispersion framework, are appeared in Fig. 5.

TABLE I. SYSTEM PARAMETERS

System quantities	Values
System fundamental frequency (f)	50Hz
Voltage source V_{s1}	11kV (L-L, rms), phase angle 0°
Voltage source V_{s2}	11kV (L-L, rms), phase angle 0°
Feeder-1 (R_{s1}+j2πfL_{s1})	Impedance : 6.05+j36.28Ω
Feeder-2 (R_{s2}+j2πfL_{s2})	Impedance : 3.05+j18.14Ω
Load L-12 Non-linear component	supplies a load of 250+j31.42Ω
Balanced load L-2 impedance	72.6+j54.44Ω

In this figure and in all the rest of the figures demonstrating three stage waveforms, the stages a, b and c are portrayed by strong, dashed and spotted lines, individually. It can be seen from Fig. 5(a) that because of the nearness of uneven and non-direct loads L-1, the voltage Vt1 is both lopsided and misshaped. Additionally, the heap L-11 causes an unbalance in the current it12 while stack L-12 causes bending in the current it11. We should now exhibit how these waveforms can be enhanced utilizing the Interline Unified Power Quality Conditioner (IUPQC).

A. IUPQC Operation

As specified some time recently, the shunt (VSC-1) holds the voltage of bus B-1 consistent. This is refined by making the VSC-1 to track a reference voltage over the filter capacitor Cf . The proportionate circuit of the VSC-1 is appeared in Fig. 6(a) in which ul.Vdc mean the inverter yield voltage where is dc capacitor voltage and u1is changing activity equivalent to (+ or – n) where n1 is turns proportion of the misfortunes and spillage inductance of the transformers are signified by Rf1 and Lf1 individually. All framework parameters are alluded to the line side of the transformers.

Defining the state space model for the VSC-1 is written as:

$$y'0=V_t'0=Hx_1 \quad (1)$$

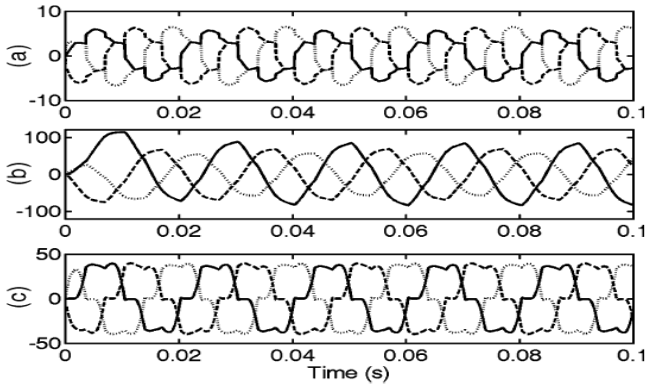

Fig. 5. Voltage & Currents in the absence of IUPQC: (a) B-1 bus voltage(V_{t1}), KV, (b) L-11 load current(i_{l11}),A, & (c) L-12 load current (i_{l12}) ,A.

Note that u_{lc} is the continuous time equivalent of u_l. The system given in (1) is discretized and is written in input–output form as:

$$A_1(z^{-1})y_1(k) = B_1(z^{-1})u_{1c}(k) + C_1(z^{-1})n_1(k) \quad (2)$$

Where n_1 is a disturbance which is equal to i_{sh}. A pole-shift controller is used to determine the switching action u_l from u_{lc}. The controller is discussed in Appendix A and is used to track a reference signal $y_{1ref}(k)$.

The reference $y_{1ref}(k)$ is the desired voltage of the bus B-1.The peak of this instantaneous voltage is pre- specified and its has angle is adjusted to maintain the power balance in the system. To set the phase angle, we note that the dc capacitor (in Fig. 4) must be able to supply VSC-1 while maintaining its dc bus voltage constant by drawing power from the ac system. A proportional controller is used for controlling the dc capacitor V_{dc} voltage and is given by

$$\delta I=K_p (V_{dcref} – V_{dcav}) \quad (3)$$

Where V_{dcav} is the average voltage across the dc capacitor over a cycle V_{dcref} is its set reference value and is the proportional gain. It is to be noted that the average voltage is obtained using a moving average low pass filter to eliminate all switching components from the signal.

TABLE II. IUPQC PARAMETERS

System quantity	Parameters
System frequency	50Hz
VSC-1 single phase transformers	1 MVA,3/11kV 10% Leakage reactance
VSC-2 single phase transformers	1 MVA,3/11kV 10% Leakage reactance
Losses	R_{f2}=1.0Ω
Leakagereactance	2πfLf1=12.1Ω 2πfLf2=12.1Ω
Filter capacitor (Cf)	50 μF
Filter capacitor (Ck)	30 μF
DC capacitor (Cdc)	3,000 μF
V_{dcref}	6.5kV

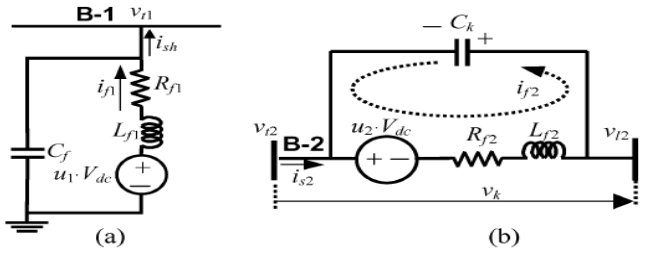

Fig. 6. Single-phase equivalent circuit of (a) VSC-1 & (b) VSC-2.

The equivalent circuit of the VSC-2 is shown in Fig. 6(b) and is similar to the one shown in Fig. 6(a) in every respect. Defining a state and input vector, respectively, as $x_2^T = [V_k \; i_{f2}]$ and $z_2^T = [u_{2c} \; i_{s2}]$.

$$x\ddot{I} = F_2x_2 + G_2z_2 \qquad y_2 = V_k = Hx_2 \qquad (4)$$

Where F_2 and G_2 are matrices that are similar to F_1 and G_1, respectively. The discrete-time input–output equivalent of (4) is given as

$$A_2(z^{-1})y_2(k) = B_2(z^{-1})u_{2c}(k) + C_2(z^{-1})n_2(k) \qquad (5)$$

Where the disturbance n_2 is equal to i_s. We now use a separate pole-shift controller to determine the switching action from so as to track the reference signal $y_{2ref}(k)$.

Note from Fig. 4 that the purpose of the VSC-2 is to hold the voltage across the sensitive load L-2 constant Let us denote the reference load L-2 voltage as V_{l2}^*. Then the reference $y_{2ref}(k)$ is computed by the application of Kirchhoff's voltage law as [see Fig. 6(b)].

$$y_{2ref} = V_{l2} \qquad t2$$

We might now exhibit the ordinary operation of the IUPQC through recreation utilizing MATLAB IUPQC parameters picked are recorded in Table II and the framework parameters are given in Table I. It can be seen from Fig. 7(a), that the three-stage B-1 voltages Vt1, are consummately adjusted with a pinnacle of 9 kV. Once these voltages get to be adjusted, the currents drawn by Feeder-1, is1, additionally get to be adjusted. The heap L-2 bus voltages Vt2, appeared in Fig. 7(c) are likewise flawlessly sinusoidal with the wanted pinnacle of (9 kV) as the converter VSC-2 infuses the required voltages in the framework. The bus B-2 voltages can be seen to have a much littler size (around 7.75 kV crest). The dc capacitor voltage Vdc is appeared in Fig. 8(a). It can be watched that it has a settling time of around 4 cycles (0.08 s) and it achieves an enduring state estimation of around 4.17 kV. The stage edge (δ1) appeared in Fig. 8(b) settles at - 33.88.

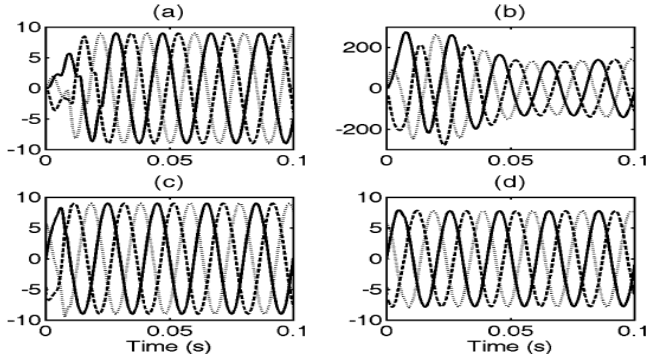

Fig. 7. System performance with an IUPQC: (a) B-1 bus voltage(V_{t1}), kv,(b)Feeder-I current(i_{s1}), A,(c) L-2 load voltage(V_{l2}), kv, (d) B-2 bus voltage(V_{t2}), kv.

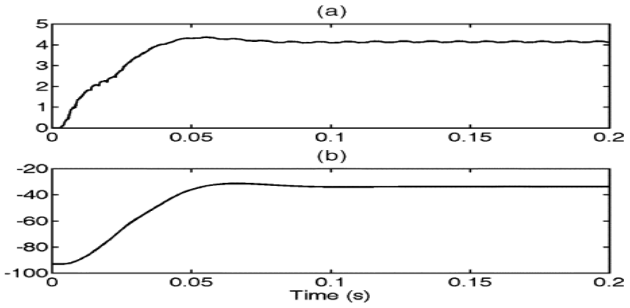

Fig. 8. (a) DC capacitor voltage (V_{dc}), kV, and (b) phase angle of B-1 bus voltage , deg.

IV. TRANSIENT PERFORMANCE OF IUPQC

A. *Voltage Sag in feeder - 1*

With the framework working in the consistent express, a 5 cycle (100ms) voltage hang happens at 0.14 s in which pinnacle of the supply voltage, lessens to 6.5 kV from their ostensible estimation of 9 kV. The different waveforms of one and only (stage an) are appeared in Fig. 9. The patterns in the other two stages are comparable. It can be seen that the dc capacitor voltage, drops when the hang happens. On the off chance that the bus voltage stays consistent, the heap power additionally lessened. Keeping in mind the end goal to supply the adjust power necessity of the heap, the drops. To balance this, the point retards with the end goal that the power provided by the source increments. As the hang is evacuated, both the voltage and stage edge comes back to their unfaltering state values. The current through Feeder-1 is additionally appeared in Fig. 9. It can be seen that with a specific end goal to supply similar load power at a decreased source voltage, the feeder current increments. Likewise, the homeless people in this current happen at the initiation and the expulsion of the droop because of the adjustment in the source voltage.

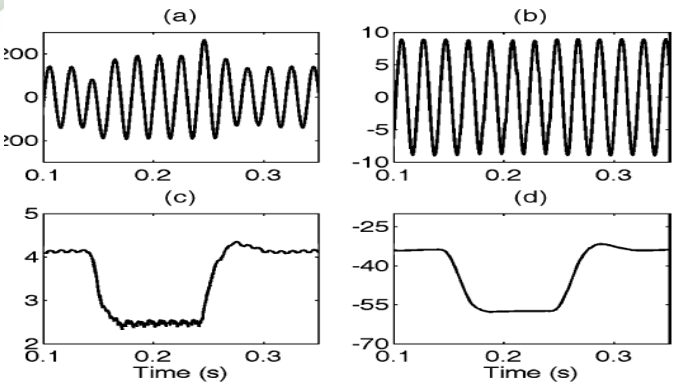

Fig. 9. System response during voltage sag in Feeder-1: (a) phase-a Feeder-1 current, A, (b) phase-a B-1 voltage, kV, (c) DC capacitor voltage (V_{dc}), kV, and (d) phase angle of B-1 bus voltage, deg.

It has been watched that bus B-1 voltage begins getting mutilated when the voltage hang makes the pinnacle of the source voltage drop beneath 6.0 kV. Additionally, for more profound voltage lists, the pinnacle of lessens and the VSC-1 is

not ready to hold the bus voltage. The following sub-segment clarifies the reason for this.

B. Voltage Sag in Feeder-2

With the framework working in the unfaltering state, Feeder-2 is subjected to a voltage hang at 0.14 s in which the pinnacle of each of the three periods of the supply voltage diminishes to 3.0 kV from their ostensible estimation of 9.0 kV. The droop goes on for 5 cycles (100 ms). The framework reaction is appeared in Figs. 10. The bus B-2 voltage, the dc interface voltage also and the edge are appeared in Fig. 10. It can be seen that vdc drops to around 2.3 kV amid the hang while v_{t1} retards to about -60 degrees.

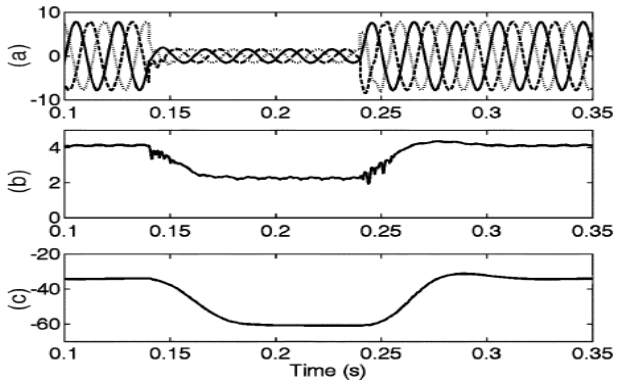

Fig. 10. (a) B-2 bus voltages (v_{t2}), kV (b) DC capacitor voltage (V_{dc}), kV, and (c) phase angle of B-1 busvoltage($v_{t\ 1}$),deg.

C. Upstream Fault in Feeder-2

The execution of the IUPQC is tried when a blame (L-G, L-L-G, and three-stage to ground) happens in Feeder-2 at bus B-2. The framework reaction is appeared in Fig. 11 when a 10 cycle L-G blame happens at 0.14 s with the end goal that the a-period of B-2 bus voltage gets to be zero. At the point when the blame happens, the power nourished to load L-2 by Feeder-2 is diminished. To meet the power necessity of the heap L-2, the dc capacitor begins providing this power immediately. This causes the dc capacitor voltage to drop from 4.1 kV to 3.5 kV. It can be seen from Fig. 11(b), that the L-2 stack voltages stay adjusted all through the blame time frame.

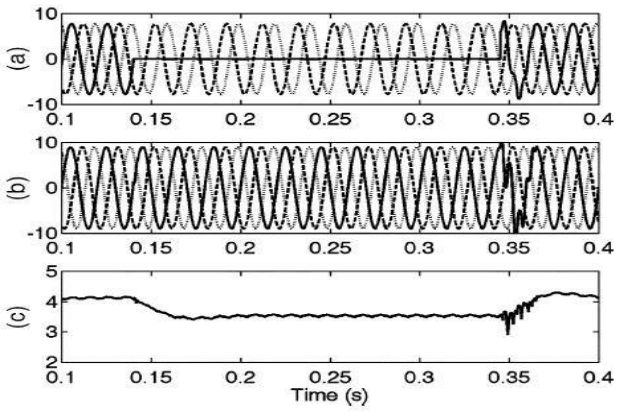

Fig. 11. System response during L-G fault at bus B-2: (a) B-2 bus voltages (v_{t2}), kV, (b) L-2 load voltages (v_{l2}), kV, and (c) DC capacitor voltage (V_{dc}), kV.

The framework reaction is appeared in Fig. 12 when a 10 cycle L-L-G blame happens at 0.14 s with the end goal that both the an and b-periods of B-2 bus voltage get to be zero. B-2 bus voltages are appeared in Fig. 12(a). It can be seen from Fig. 12(b), that the L-2 stack voltages stay adjusted. Nonetheless, the dc capacitor voltage now drops to around 2.65 kV and v_{t1} from -34 deg to -55 deg. Still it is enough to regulate both the load voltages.

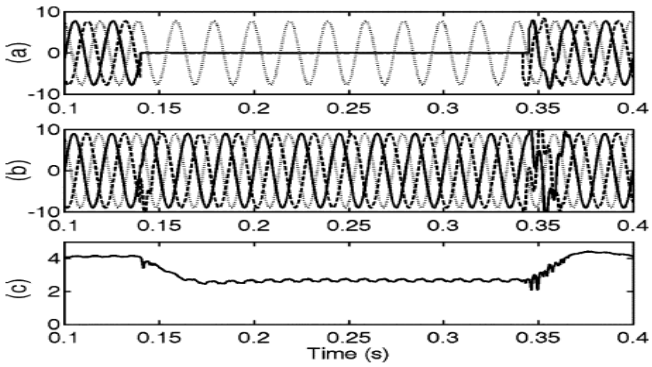

Fig. 12. System response during L-L-G fault at bus B-2 (a) B-2 bus voltages (v_{t2}), kV, (b) L-2 load voltages (v_{l2}), kV, and (c) DC capacitor voltage (V_{dc}), kV.

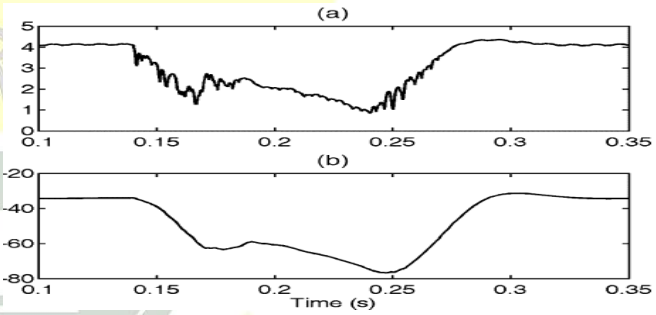

Fig. 13. (a) DC capacitor voltage (V_{dc}), kV, and (b) phase angle of B-1 bus voltage ($\delta 1$) in deg. for a fault at B-2.

Presently, the framework execution has been tried when a three stage blame happens at 0.14 s in Feeder-2 at bus B-2 with the end goal that the voltage gets to be zero. The framework reaction is appeared in Figs.13 and 14 where the blame is accepted to last 5 cycles as it were. At the point when the blame happens, the power encouraged to load L-2 by Feeder-2 gets to be zero. To meet the power prerequisite of the heap L-2, the dc capacitor begins providing this power quickly. This causes the dc capacitor voltage to drop and, to counterbalance the voltage drop, the point impedes. Subsequently, power is drawn from the source through Feeder-1 and provided to both the heaps L-1 and L-2. These two amounts recover their ostensible unfaltering state values once the blame is cleared. This is apparent from Fig.13.

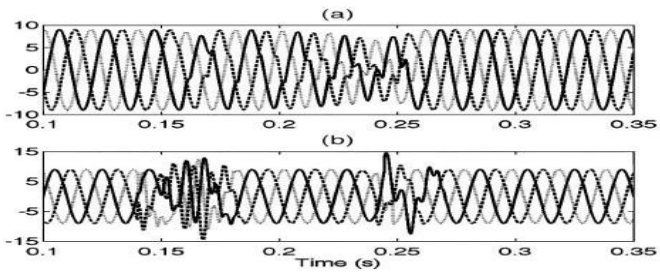

Fig. 14. (a) B-1 bus voltages (v_{t1}), kV and (b) L-2 load voltages (v_{l2}) in kV for a fault at bus B-2.

The bus B-1 voltage and the heap L-2 voltage are appeared in Fig.14. It can be seen that notwithstanding drifters toward the starting and toward the end of the blame, the voltage over the touchy load stays adjusted and sinusoidal. Nonetheless, since the point drops beneath - 75 deg, the bus B-1 voltage gets bended and its extent likewise diminishes. These voltages, in any case, recapture their ostensible values inside a cycle of the evacuation of the blame.

V. FUZZY LOGIC CONTROLLERS

The word Fuzzy means vagueness. Fuzziness occurs when the boundary of piece of information is not clear-cut. In 1965 Lotfi A.Zahed propounded the fuzzy set theory. Fuzzy set theory exhibits immense potential for effective solving of the uncertainty in the problem. Fuzzy set theory is an excellent mathematical tool to handle the uncertainty arising due to vagueness. Understanding human speech and recognizing handwritten characters are some common instances where fuzziness manifests. Fuzzy set theory is an extension of classical set theory where elements have varying degrees of membership. Fuzzy logic uses the whole interval between 0 and 1 to describe human reasoning. In FLC the input variables are mapped by sets of membership functions and these are called as "FUZZY SETS".

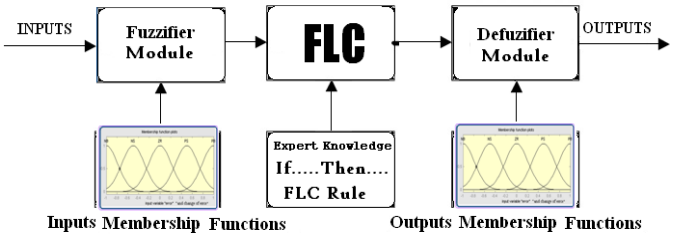

Fig. 15. Fuzzy Basic Module.

Fuzzy set comprises from a membership function which could be defines by parameters. The value between 0 & 1 reveals a degree of membership to the fuzzy set. The process of converting the crisp input to a fuzzy value is called as "fuzzification". The output of the fuzzier module is interfaced with the rules. The basic operation of FLC is constructed from fuzzy control rules utilizing the values fuzzy sets in general for the error, change of error & control action. The results are combined to give a crisp output, controlling the output variable and this process is called "defuzzification".

e|Δe	NB	NM	NS	Z	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	Z
NM	NB	NB	NB	NM	NS	Z	PS
NS	NB	NB	NM	NS	Z	PS	PM

Fig. 16. Control Strategy based on 49 Fuzzy control rules with combination of seven error states multiplying with seven changes of error states.

VI. MATLAB DESIGN OF CASE STUDY & RESULTS

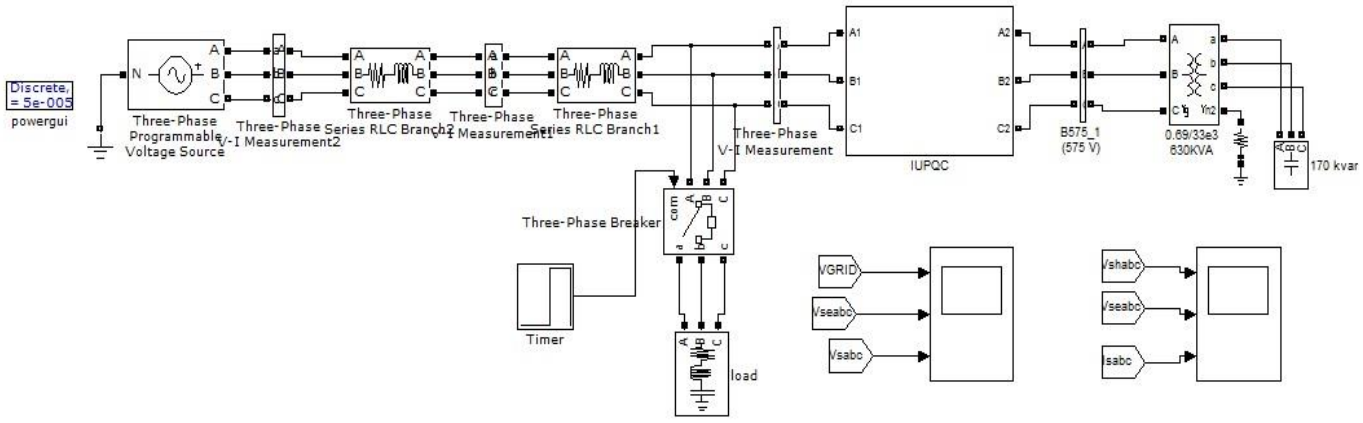

Fig. 17. Simulink model of IUPQC.

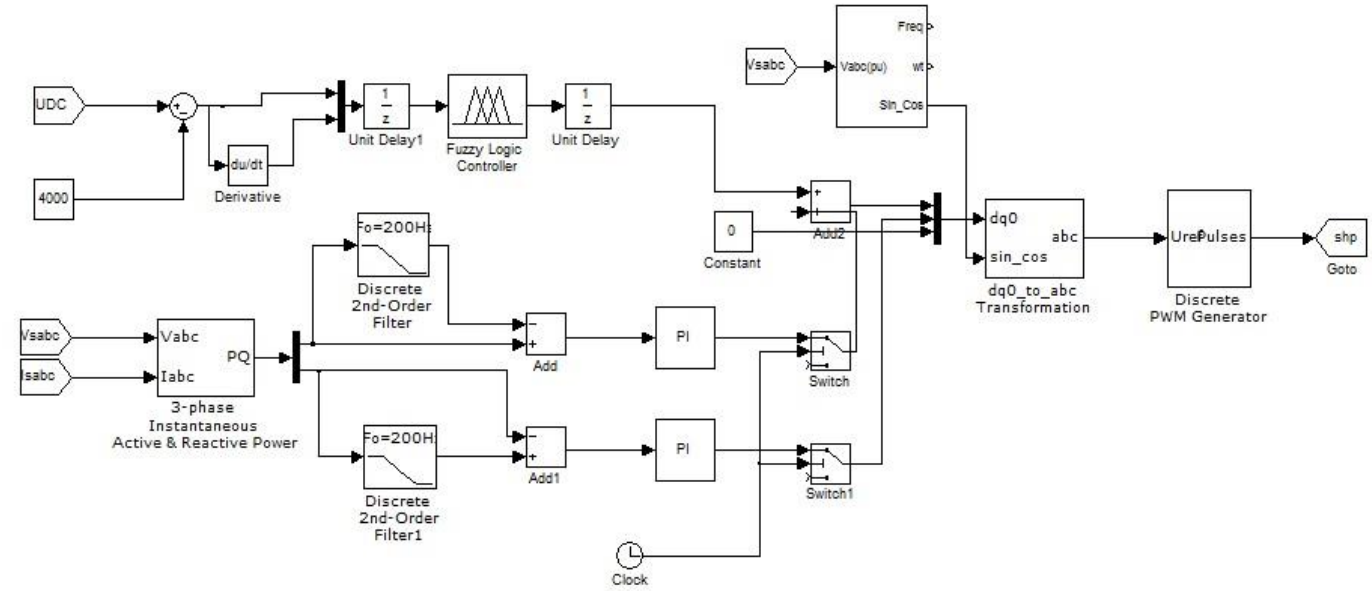

Fig. 18. Simulink model of IUPQC with FLC.

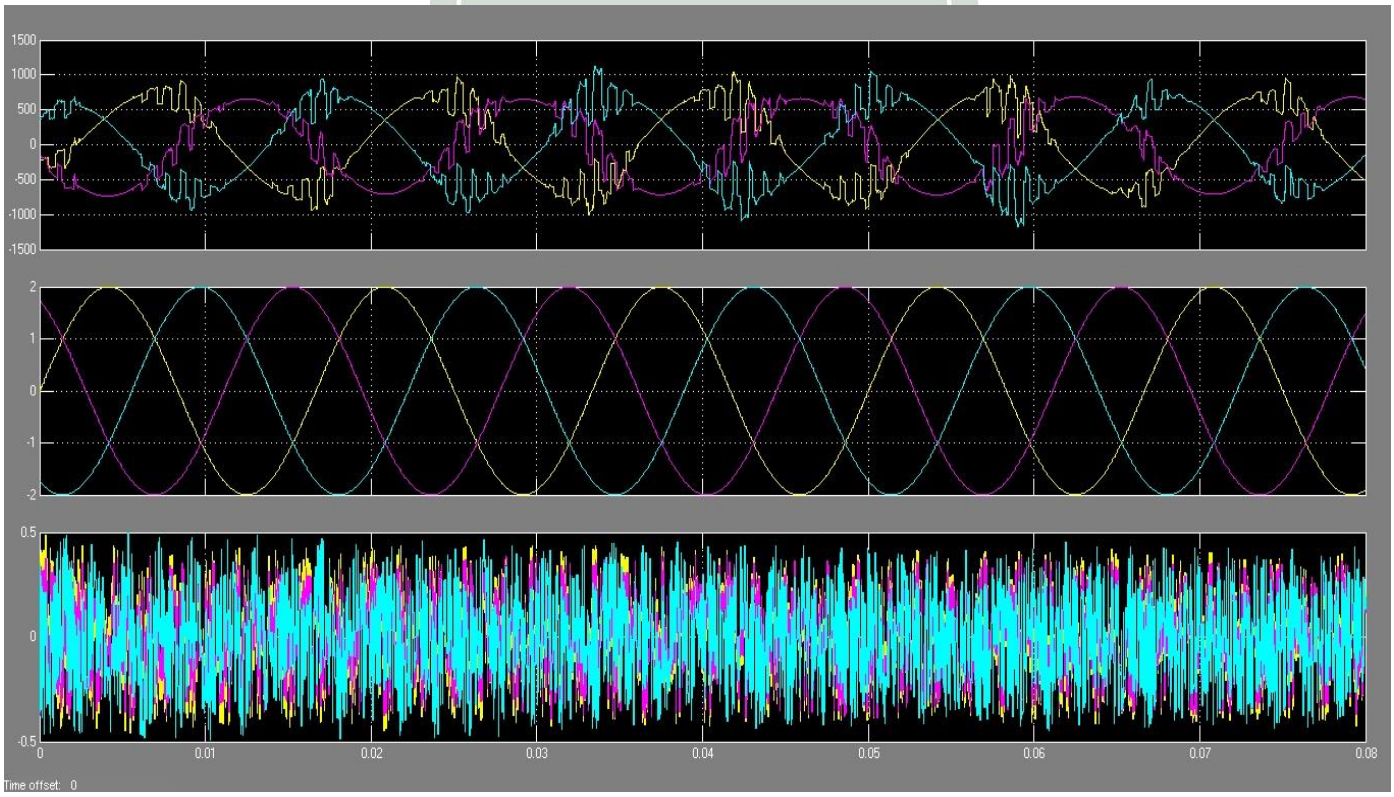

Fig. 19. Simulink results without FLC.

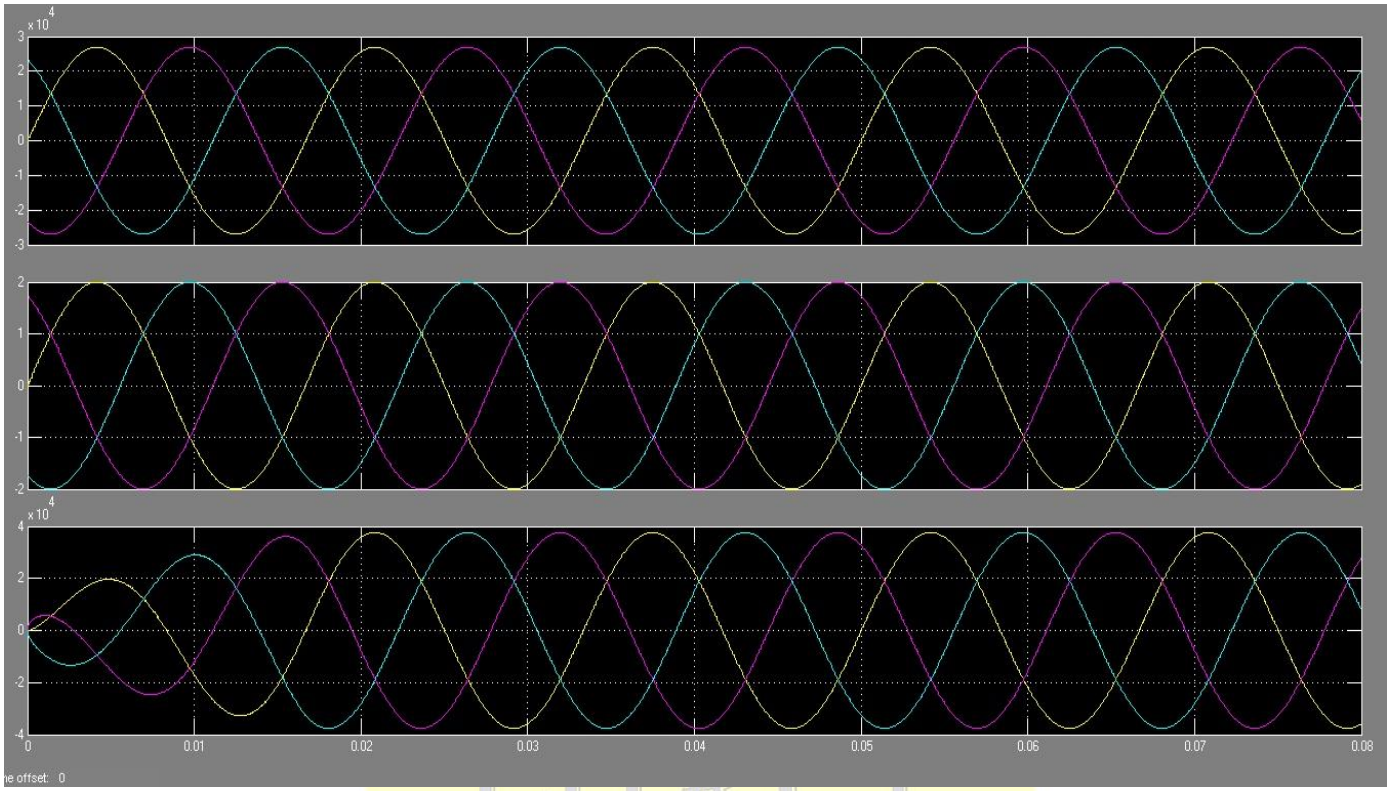

Fig. 20. Simulink results with FLC.

CONCLUSION

In the enhanced iUPQC controller, the currents integrated by the arrangement converter are dictated by the normal dynamic power of the heap and the dynamic power to give the dc-connect voltage direction, together with a normal responsive power to manage the lattice bus voltage. In this way, notwithstanding all the power-quality pay components of a customary UPQC or an iUPQC, this enhanced controller additionally impersonates a STATCOM to the network bus. This new component improves the appropriateness of the iUPQC and gives new arrangements in future situations including brilliant frameworks and microgrids, including disseminated era and energy stockpiling systems to better manage the inborn fluctuation of renewable assets, for example, sunlight based and wind power. In addition, the enhanced iUPQC controller may legitimize the costs and advances the iUPQC materialness in power quality issues of basic systems, where it is fundamental an iUPQC or a STATCOM, as well as both, at the same time. Notwithstanding the expansion of one more power-quality remuneration include, the framework voltage control decreases the inward circle coursing power inside the iUPQC, which would permit bring down power rating for the arrangement converter. The trial comes about checked the enhanced iUPQC objectives. The framework voltage control was accomplished with no heap, and additionally when providing a three-stage nonlinear load. These outcomes have shown a reasonable execution of voltage control at both sides of the iUPQC, even while remunerating consonant current and voltage lopsided characteristics.

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